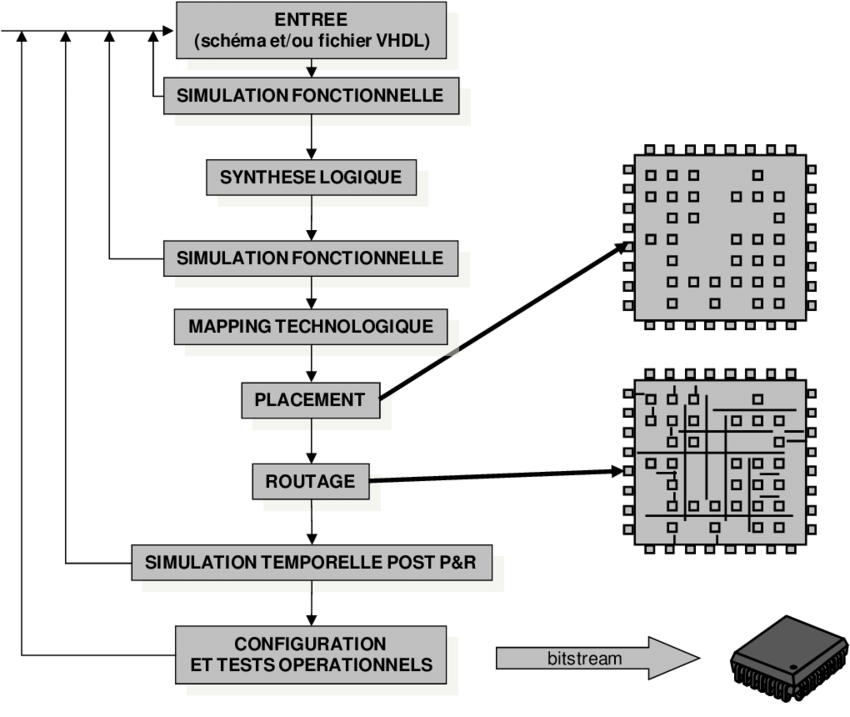
Numérique

FPGA :

Xillinx vivado :

* edit rtl descripton in VHDL or Verilog
* simulate
* synthetysis
* implementation
* generate bitstream

report and summary to look at TNS (total negative slack), critical path, ressources used (LUT…etc) and help to improve rtl description to enhance ressources use



ASIC

Synthesis : Design vision

Simu (bhv,post\_syn,post\_par) : Modelsim

PAR : EDI by Cadence

